MAX114/118

Integrated Circuits
Special Function

ELEKTOR ELECTRONICS
DATASHEET 11/2000

Electrical Characteristics

(V_{DD} = +5V ±5%, REF+ = 5V, REF– = GND, Read Mode (MODE = GND), T_A = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	N		8			Bits
Total Unadjusted Error	TUE				±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Zero-Code Error					±1	LSB
Full-Scale Error					±1	LSB
Channel-to-Channel Mismatch					±1/4	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Plus Distortion Ratio	SINAD	MAX11_C/E, fSAMPLE = 1MHz, fIN_ = 195.8kHz	45			dB
		MAX11_M, fSAMPLE = 740kHz, fIN_ = 195.7kHz	45			
Total Harmonic Distortion	THD	MAX11_C/E, fSAMPLE = 1MHz, fIN_ = 195.8kHz			–50	dB
		MAX11_M, fSAMPLE = 740kHz, fIN_ = 195.7kHz			–50	
Spurious-Free Dynamic Range	SFDR	MAX11_C/E, fSAMPLE = 1MHz, fIN_ = 195.8kHz	50			dB
		MAX11_M, fSAMPLE = 740kHz, fIN_ = 195.7kHz	50			
Input Full-Power Bandwidth		$V_{IN\_}$ = $5V_{p-p}$		1		MHz
Input Slew Rate, Tracking			3.1	15		V/ms
ANALOG INPUT						
Input Voltage Range	VIN_		V_{REF-}		V_{REF+}	V
Input Leakage Current	IN	GND < $V_{IN\_}$ < V_{DD}				µA
Input Capacitance	CIN_			32		pF
REFERENCE INPUT						
Reference Resistance	RREF		1	2	4	kΩ
REF+ Input Voltage Range			V_{REF-}		V_{DD}	V
REF– Input Voltage Range			GND		V_{REF+}	V

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MAX114/MAX118

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1µA Power-Down

Manufacturer

Maxim Integrated Products. Internet: http://www.maxim-ic.com

Application Example

Gameboy Digital Sampling Oscilloscope (GBDSO), Elektor Electronics October & November 2000

General Description

The MAX114/MAX118 are microprocessor-compatible, 8-bit, 4-channel and 8-channel analog-to-digital converters (ADCs). They operate from a single +5V supply and use a half-flash technique to achieve a 660ns conversion time (1Msps). A power-down (PWRDN) pin reduces current consumption typically to 1µA. The devices return from power-down mode to normal operating mode in less than 200ns, allowing large supply-current reductions in burst-mode applications (in burst mode, the ADC wakes up from a low-power state at specified intervals to sample the analog input signals). Both converters include a track/hold, enabling the ADC to digitize fast analog signals. Microprocessor (µP) interfaces are simplified because the ADC can appear as a memory location or I/O port without external interface logic. The data outputs use latched, three-state buffer circuitry for direct connection to an 8-bit parallel µP data bus or system input port. The MAX114/MAX118 input/reference configuration enables ratiometric operation.

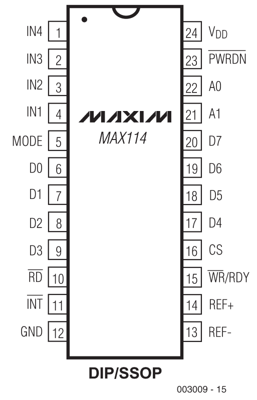
The 4-channel MAX114 is available in a 24-pin DIP or SSOP. The 8-channel MAX118 is available in a 28-pin DIP or SSOP.

Applications

High-Speed DSP
Remote Data Acquisition
Portable Equipment
Communications Systems

Features

- Single +5V Supply Operation
- 4 (MAX114) or 8 (MAX118) Analog Input Channels
- Low Power:
  40mW (operating mode)
  5µW (power-down mode)
- Total Unadjusted Error £1LSB
- Fast Conversion Time: 660ns per Channel
- No External Clock Required
- Internal Track/Hold
- 1MHz Full-Power Bandwidth
- Internally Connected 8th Channel Monitors Reference Voltage (MAX118)



MAX114 Pin Configuration

Ordering Information

PART	TEMP. RANGE	PIN PACKAGE
MAX114CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX114CAG	0°C to +70°C	24 SSOP
MAX114C/D	0°C to +70°C	Dice
MAX114ENG	–40°C to +85°C	24 Narrow Plastic DIP
MAX114EAG	–40°C to +85°C	24 SSOP
MAX114MRG	–55°C to +125°C	24 Narrow CERDIP

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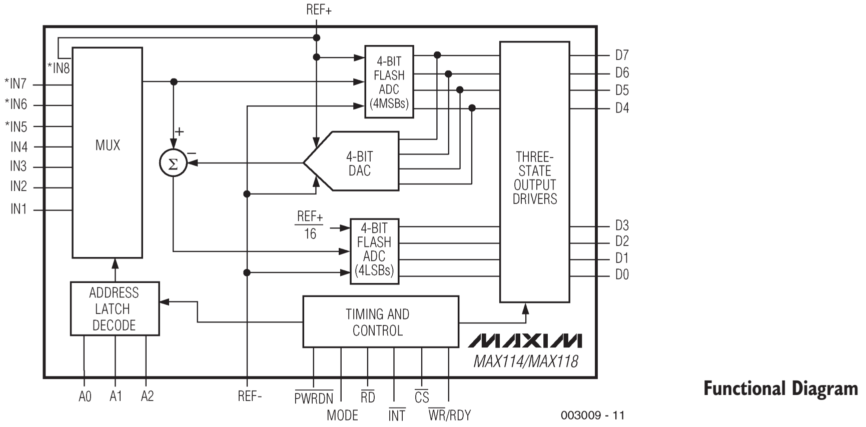
Pin Description (MAX114 only)

Pin	Name	Function
1	IN4	Analog Input Channel 4
2	IN3	Analog Input Channel 3
3	IN2	Analog Input Channel 2
4	IN1	Analog Input Channel 1
5	MODE	Mode Selection Input. Internally pulled low with a 50 µA current source. MODE = 0 activates read mode; MODE = 1 activates write-read mode.
6	D0	Three-State Data Output (LSB).
7, 8, 9	D1, D2, D3	Three-State Data Outputs.
10	$\overline{\text{RD}}$	Read Input. $\overline{\text{RD}}$ must be low to access data.
11	$\overline{\text{INT}}$	Interrupt Output. $\overline{\text{INT}}$ goes low to indicate end of conversion.
12	GND	Ground
13	REF–	Lower Limit of Reference Span. REF– sets the zero-code voltage. Range is GND ≤ $V_{REF-} < V_{REF+}$.
14	REF+	Upper Limit of Reference Span. REF+ sets the full-scale input voltage. Range is $V_{REF-} < V_{REF+} \leq V_{DD}$. Internally hard-wired to IN8.
15	$\overline{\text{WR}}$/RDY	Write-Control Input/Ready-Status Output.
16	$\overline{\text{CS}}$	Chip-Select Input. $\overline{\text{CS}}$ must be low for the device to recognize $\overline{\text{WR}}$ or $\overline{\text{RD}}$ inputs.
17, 18, 19	D4, D5, D6	Three-State Data Outputs.
20	D7	Three-State Data Output (MSB).
21	A1	Multiplexer Channel Address Input.
22	A0	Multiplexer Channel Address Input (LSB)
23	$\overline{\text{PWRDN}}$	Power-Down Input. $\overline{\text{PWRDN}}$ reduces supply current when low.
24	V_{DD}	Positive Supply, +5V.



Functional Diagram

MAX114/118

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2		2.4			V
		MODE		3.5			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				0.8	V
		MODE				1.5	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				±1	µA
		$\overline{WR}$				±3	
		MODE			50	200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				±1	µA
Input Capacitance (Note 2)	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA, INT, D0–D7				0.4	V
		RDY, I_{SINK} = 2.6mA				0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 360µA, INT, D0–D7		4			V
Three-State Current	I_{LKG}	D0–D7, RDY, digital outputs = 0V to V_{DD}				±3	µA
Three-State Capacitance (Note 2)	C_{OUT}	D0–D7, RDY			5	8	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
V_{DD} Supply Current	I_{DD}	$\overline{CS} = \overline{RD}$ = 0V, $\overline{PWRDN} = V_{DD}$	MAX11_C		8	15	mA
			MAX11_E/M		8	20	
Power-Down V_{DD} Current		$\overline{CS} = \overline{RD} = V_{DD}$, $\overline{PWRDN}$ = 0V (Note 3)			1	10	µA
Power-Supply Rejection	PSR	V_{DD} = 4.75V to 5.25V, V_{REF} = 4.75V			±1/16	±1/4	LSB

Note 2: Guaranteed by design.
Note 3: Power-down current increases if logic inputs are not driven to GND or VDD